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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,976	09/19/2003	Peter J. Barry	10559-849001 /INTEL P1687	5368

20985	7590	01/17/2007

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EXAMINER
WALTER, CRAIG E

ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

	Application No.	Applicant(s)
Office Action Summary	10/665,976	BARRY ET AL.
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>13 November 2006</u>.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-51</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-51</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)	5) ☐ Notice of Informal Patent Application
Paper No(s)/Mail Date _____ .	6) ☐ Other: _____ .

DETAILED ACTION

Status of Claims

1.   Claims 1-51 are pending in the Application.

Claims 1, 7,13, 18, 24, 29, 34, 39, 43 and 47 are amended.

Claim 51 is new.

Claims 1-51 are rejected.

Response to Amendment

2.   Applicant's amendments and arguments filed on 13 November 2006 in response

to the office action mailed on 10 August 2006 have been fully considered, but they are

not persuasive. Therefore, the rejections made in the previous office action are

maintained, and restated below, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1-3, 5, 7-8, 10-11, 13-14, 16, 18-19, 21-22, 24-26, 39-40, 42-44, and 46-

49 are rejected under 35 U.S.C. 102(e) as being anticipated by Qureshi et al. (US PG

Publication 2004/0030856 A1), hereinafter Qureshi.

As for claims 1, 13, and 47, Qureshi teaches a method comprising:

from at least two types of endian conversion, including a first type, which

can be performed on a portion of data (page) stored within a memory system and

a second type which can be performed on the same portion of data stored within

the memory system, determining a type (two types of conversion may be

performed on the data by remapping the most significant and least significant bits

(i.e. big-to-little, or little-to-big) - paragraphs 0004 and 0005, all lines. The

determination for swapping occurs via the indicator stored in the endian selection

register which is based on the determination the OS type) — see also Fig. 6

(step 607 discloses little endian conversion, and step 609 discloses big endian

conversion – paragraphs 0022 and 0023, all lines); and

writing an entry to a memory management table based on the determining

(based on the determination of what type of conversion can be performed based

on the OS type, the endian selection register is written to designate which type of

swapping is required - paragraphs 0022 and 0023, all lines).

As for claims 7 and 18, Qureshi teaches a method (and product) comprising:

maintaining a memory management table that includes one or more

entries, each entry defining a location of a portion of data stored within a memory

system and indicating a type determined from at least two types of endian conversion,

including a first type which can be performed on the portion of data stored within the

memory system and a second type which can be performed on the same portion of data

stored within the memory system (referring to Fig. 5 and paragraph 0018, all lines, the

system event registers (SER) comprise information which stores both what type of

endian conversion can be performed (stored in the endian selection register), and

address decode logic to define the location of the data itself. As discussed in the

rejection of claim 1, Fig. 6 defines the process of setting the register to determine which

conversion can be performed, and how each of the two conversion types are actually

carried out – paragraphs 0022-0023, all lines).

As for claim 24, Qureshi teaches a memory management table residing in

computer memory comprising:

one or more table entries, with each table entry having a first field for

defining the location of a portion of data stored within a memory system and a

second field for defining a type determined from at least two types of endian

conversion, including a first type which can be performed on the portion of data

stored within a memory system and a second type which can be performed on

the same portion of data stored within the memory system (referring to Fig. 5,

and paragraph 0018, all lines; the type of conversion, as well as the location of

the data that corresponds to the type of conversion are stored as separate fields

in the system event registers to allow the system to access, and swap the

necessary data).

As for claims 39 and 43, Lasserre teaches a method (and product) comprising:

accessing a table entry of a memory management table, wherein the table

entry is associated with a portion of data stored within a memory system and includes

a conversion-type indicator (Fig. 5, paragraph 0018, all lines - the endian selection

register (storing the conversion indicator) is accessed to perform the appropriate

endian conversion); and

from at least two types of endian conversion, including a first type which

can be performed on the portion of data stored within a memory system and a second

type which can be performed on the same portion of data stored within the memory

system, determining a type based on the conversion-type indicator (as discussed in the

rejection of claim 1 presented *supra*).

As for claims 5, 10, 16, 21, 25, 42 and 46, Qureshi teaches the entry as including

a single bit for specifying one of two types of endian conversion (paragraph 0004, all

lines).

As for claims 2 and 48, Qureshi teaches writing an entry to a memory

management table as further including specifying the location of the portion of data

within the memory system (paragraph 0018, all lines- the SER stores data indicating

the location of the data to be converted).

As for claims 3, 8, 14, 19, 26, 40, 44 and 49, Qureshi discloses the at least two

types of endian conversion as including a data coherent conversion type (Fig. 6

illustrates the conversion as occurring by swapping the least and most significant

bytes. Byte swapping is the same procedure as data coherent type conversion as both

aim to reverse the order of the bytes within a word in order to convert from big/little

endian formats).

As for claims 11 and 22, Qureshi teaches the portion of the data as being stored

at a physical memory address within the memory system (paragraph 0018, all lines –

the data is obtained via the physical address which is accomplished via the selection

signal in the SER).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 6, 12, 17, 23, 28, 29-30, 32-35, and 37-38 are rejected under 35 U.S.C.

103(a) as being unpatentable over Qureshi (US PG Publication 2004/0030856 A1) as

applied to claims 1, 7, 13, 18, 24, in further view of Lasserre et al., (US PG Publication

2002/0069339 A1) hereinafter Lasserre.

As for claims 29 and 34, Qureshi teaches a system (and architecture)

comprising:

an endian converter for converting portions of data from the first endian

format to the second endian format (paragraphs 0022-0023, all lines – the system is

capable of performing either a big or little endian conversion based on the information

stored in the register); and

a memory management table including one or more entries, with each entry

defining a location for a portion of data stored within a memory system to be converted

from the first endian format to the second endian format, and indicating a type

determined from at least two types of endian conversion, including a first type which

can be performed on the portion of data stored within the memory system by the

endian converter and a second type which can be performed on the same portion of

data within the memory system (referring to Fig. 5, and paragraph 0018, all lines; the

type of conversion, as well as the location of the data that corresponds to the type of

conversion are stored as separate fields in the system event registers to allow the

system to access, and swap the necessary data).

Despite these teachings Qureshi fails to teach the remaining limitations of these

claims.

Lasserre does in fact teach the remaining limitations, including:

a networking device (Fig. 8 illustrates the system as being implemented

on a wireless networking device – paragraph 0083, all lines), including:

a first processor for processing data in a first endian format (Fig. 4,

element 402 – little endian processor);

a second processor for processing data in a second endian format (Fig. 4,

element 400, big endian processor);

a bus for interconnecting the first and second processors (paragraph

0065, lines 1-8 - both processors are wired to a data bus);

As for claims 6, 17, and 28, Lasserre teaches mapping a virtual memory address

to a physical memory address (paragraph 0060, lines 1-3, each entry in the TLB maps

a physical address with every corresponding virtual address).

As for claims 12 and 23, Lasserre teaches the entry as mapping the physical

address at which the portion of data is stored to a virtual address accessible by a

processor (paragraph 0060, lines 1-3, each entry in the TLB maps a physical address

with every corresponding virtual address. The processor is able to access the

addresses via the TLB as further described in paragraph 0029, line 1 through paragraph

30, line 8 – The TLB contains entries for virtual-to-physical address translation which is

accessible by the MMU containing the processor core/s).

As for claims 32 and 37, Lasserre teaches the first processor as being a little-

endian processor (Fig. 4, element 402 – paragraph 0065, lines 1-2).

As for claims 33 and 38, Lasserre teaches the second processor as being a big-

endian processor (Fig. 4, element 400 – paragraph 0065, lines 1-2).

It would have been obvious to one of ordinary skill in the art at the time of the

invention for Qureshi to further include Lasserre's system with MMU descriptor having a

big/little end bit to control the transfer of data between devices into his own system and

method for operating in endian independent mode. By doing so, Qureshi would be able

to exploit the benefit of utilizing more than one processor (including a DSP for example)

which could greatly improve the performance of his system as taught by Lasserre in paragraph 0004, all lines.

As for claims 30 and 35, Qureshi discloses the at least two types of endian conversion as including a data coherent conversion type (Fig. 6 illustrates the conversion as occurring by swapping the least and most significant bytes. Byte swapping is the same procedure as data coherent type conversion as both aim to reverse the order of the bytes within a word in order to convert from big/little endian formats).

5.   Claims 4, 9, 15, 20, 27, 41, 45, 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Qureshi (US PG Publication 2004/0030856 A1) as applied to claims 1, 7, 13, 18, 24, 39, 43, and 47, and in further view of Ikumi (US Patent 5,630,084).

As for claims 4, 9, 15, 20, 27, 41, 45, 50 and 51 the Qureshi fails to teach endian conversion as being address coherent. Ikumi however teaches a system for converting data in little endian to big endian and vice versa by reversing two bits of address referencing one word of four words. In his disclosure, Ikumi teaches reversing the bits of the byte address in order to convert data from big-little (and vise versa) endian format (col. 4, lines 9-21 – Also referring to Fig. 6, byte address reversal is disclosed). Note Ikumi's system of address reversal for endian conversion is the same as the "address coherent conversion" as shown in Table 1, page 3 of Applicant's specification. It would have been obvious to one of ordinary skill in the art at the time of the invention for Qureshi to utilize Ikumi's system of endian conversion through address conversion,

in addition to his byte swapping endian conversion method. By doing so, Qureshi would

be able to exploit the benefits of using an additional form of endian conversion (i.e.

address coherent), which overcomes the draw backs of traditional byte swapping

(switching) method which severely complicates operational control during processing of ·

the data (Ikumi – col. 2 – lines 38-46). Ikumi further discusses how the address

coherent method overcomes drawbacks of the swapping method in col. 2, lines 48-62 of

his disclosure (i.e. operational control of the data processing is markedly improved). ·

6.   Claims 31 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable

over the combined teachings of Qureshi (US PG Publication 2004/0030856 A1), and

Lasserre (US PG Publication 2002/0069339 A1) as applied to claims 29 and 34, and in

further view of Ikumi (US Patent 5,630,084).

As for claims 31 and 36, the combined teachings of Qureshi and Lasserre fail to

teach endian conversion as being address coherent. Ikumi however teaches a system

for converting data in little endian to big endian and vice versa by reversing two bits of

address referencing one word of four words. In his disclosure, Ikumi teaches reversing

the bits of the byte address in order to convert data from big-little (and vise versa)

endian format (col. 4, lines 9-21 – Also referring to Fig. 6, byte address reversal is

disclosed). Note Ikumi's system of address reversal for endian conversion is the same

as the "address coherent conversion" as shown in Table 1, page 3 of Applicant's

specification.

It would have been obvious to one of ordinary skill in the art at the time of the

invention for Qureshi to utilize Ikumi's system of endian conversion through address

conversion, in addition to his byte swapping endian conversion method. By doing so, Qureshi would be able to exploit the benefits of using an additional form of endian conversion (i.e. address coherent) which overcomes the draw backs of traditional byte swapping (switching) method which severely complicates operational control during processing of the data (Ikumi – col. 2 – lines 38-46). Ikumi further discusses how the address coherent method overcomes drawbacks of the swapping method in col. 2, lines 48-62 of his disclosure (i.e. operational control of the data processing is markedly improved).

Response to Arguments

7.   Applicant's arguments filed 13 November 2006 have been fully considered but they are not persuasive.

With respect to newly amended claim 1, Applicant asserts Qureshi's disclosure fails to anticipate all limitations of the claim because it allegedly discloses; "a portion of data that is big-endian [that] would always undergo a big-to-little conversion, and a portion of data that is big-endian [that] would always undergo a little-to-big conversion. Applicant concludes, "both types of endian conversion (big-to-little and little-to-big) would not be performed on the same portion of data. Therefore, Qureshi does not disclose and would not have suggested determining a type "from at least two types of endian conversion, including a first type which can be performed on a portion of data stored within a memory system and a second type which can be performed on the same portion of data..." as recited in claim 1."

This argument however is not persuasive as Applicant's remarks and arguments are not commensurate with the scope of the claim limitation. The claim requires, *inter alia*, "a first type [of data] which *can* be performed on a portion of data ... and a second type which *can* be performed on the same portion of data..." (emphasis added). Applicant argues that Qureshi fails to teach performing both types of conversion on the same portion of data, however the limitation only requires performing one type (i.e. "determining a type" as per claim 1). The thrust of Qureshi's invention is to have the ability to perform the necessary conversion of data to accommodate multiple operating systems (paragraphs 0004 through 0005, all lines). In other words, Qureshi's system is intended to be flexible in order to convert data to result in data being stored in big endian format, convert data to result in data being stored in little endian format, hence the system is flexible such that it *can* perform either type of conversion. See also Fig. 6, which discloses either mapping the LSB or MSB to the lowest address based on the determination at step 605. This figure clearly illustrates that either conversion *can* be performed on the data

Further, assuming *arguendo* that Applicant's aforementioned narrow interpretation of the newly amended claim limitation is correct (i.e. requiring both types of conversion to be *actually* performed), Examiner maintains that Qureshi still anticipates this claim limitation. Referring again to paragraphs 0004 through 0005, all lines, Qureshi teaches performing the necessary conversion of data upon system boot. Appropriate conversions take place *on the same data* each time the system is booted,

and are adjusted according the needs of each of the operating systems during a respective system boot.

Applicant's argument that the remaining independent and dependant claims are allowable for at least similar reasons as claim 1 is rendered moot, as Examiner maintains all rejections to the pending claims per the arguments and rejections discussed *supra*.

Conclusion

8.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
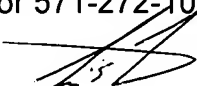
9.   A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

11.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

12.   Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

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USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

1-11-07